Supplemental Assignment

Part 1

Brian Burke

18322240

Q.1

CISC stands for “Complex Instruction Set Computing”. The CISC processor architecture contains a large set of computer instructions that range from simple to complex and extremely specialized. The idea behind the CISC approach is to minimize the number of instructions per program which inevitably results in the sacrifice of increasing the number of cycles per instruction. Computers based on the CISC processor architecture are designed to decrease the memory cost. As large programs require more storage, this increases the memory cost. To solve this, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thus increasing their complexity. The clear advantages of the CISC approach is that microprogramming is an easy assembly language to implement, and less expensive than hard wiring a control unit. In addition, micro coding new instructions is simple and thus it allows designers to make CISC machines upwardly compatible. Finally, as each instruction becomes more functional, less instructions are needed to complete a given task. One of the disadvantages of the CISC processor architecture is that the performance of the machine slows down due to the differing time lengths being taken by different instructions. Furthermore, only about 20% of the existing instruction set is typically used in any given program, despite there being many specialised instructions to complete the task. Finally, the conditional codes are set by the CISC instructions, which must be examined by the complier each time before a subsequent instruction can be executed, causing delays.

RISC stands for “Reduced Instruction Set Computing”. RISC processors have fewer instructions and fewer addressing nodes. The instruction set is much less and more straightforward and are combined to execute more complex commands. RISC is a type of microprocessor architecture that uses a highly optimized set of instructions. RISC uses the Harvard memory model and as such it is the Harvard architecture. RISC is designed to carry out a small number of instructions at any given time. RISC utilises a complex compiler to convert the high-level language statement into the code of its form. Any RISC register can be used in many different contexts. RISC has many of these registers to prevent memory activity. Pipelining is one of the unique features of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. As such, it has a high-performance advantage over CISC. Another advantage is that fewer instructions also imply fewer transistors required. RISC is favoured in portable devices due to its power efficiency. The chips for RISC are cheaper to design and produce as they require fewer transistors. Additionally, the level of decoding required is lower. Some disadvantages of the RISC processor include the fact that its performance is heavily dependent on compiler or programmer. Another disadvantage is the large memory cache required on the chip itself. A final disadvantage of RISC is the unfortunate requirement for continuous on-chip hardware reprogramming.

VLIW stands for “Very long instruction word”. This type of processor architecture involves a pre-processor or language compiler which decodes program instructions into simple operations which can be performed by the processor simultaneously. These simple instructions are organised into a very long instruction word which the processor can handle and direct to its correct functional unit. VLIW is often viewed as the next step beyond RISC as both operate on a limited set of basic instructions. Some advantages of VLIW include the reduction in hardware complexity and power consumption. It also increases the potential clock time. Additionally functional units are now positioned corresponding to the instruction pocket by the compiler. The added disadvantages to VLIW processor architecture include the fact that more complex compilers are necessary, which are difficult to design, there is an increase in the program code size, and a larger memory bandwidth and register-file bandwidth. In addition, cache misses and other unscheduled events which lead to a stall become more likely. There is also waste involved with memory space and instruction bandwidth regarding un-filled operation codes.

Q.2

A processor stack is the location where some instructions store or retrieve certain data. When an interrupt such as a PUSH, POP, CALL, RETURN or INT occurs, it is where data is stored. It is also used to store the status register contents before a context switch.

The processor stack is a useful concept in microprocessor architecture as it allows for the efficient computation of complex arithmetic expressions. Furthermore, the speed of instruction execution is rapid due to operand data being stored in consecutive memory locations. Another benefit is that the length of instructions is shorter than would otherwise be possible as they do not necessitate an address field.

The system in the Cortex M0+ is controlled by the system control registers which are only accessible through word transfers. Each of these registers is 32 bits wide.

The processor in the Cortex M0+ implements two stacks, namely the main stack and the process stack, with independent copies of the stack pointer. The processor has two modes, the Thread mode and the Handler mode. The use of the main stack or the process stack by the processor in Thread mode is determined by the CONTROL register. The main stack is always used in Handler mode. Thread mode is utilised to execute applications, whereas Handler mode is used to execute exception handlers.

Q.3

CPU pipelining is the overlapping of instructions inside of the CPU. This is achieved by fetching the next instruction before the current instruction is fully executed.

The advantages of CPU pipelining include the following, an increase in the overall performance of the CPU, an increase in the instruction throughput, and the design of a faster ALU becomes possible.

One disadvantage of CPU pipelining is that designing a pipelined processor is very much an expensive and complex process. The instruction latency is also higher.

Pipeline Control Hazards originate from the pipelining of branches and instructions which alter the PC. They can cause a great performance loss in the efficiency of the CPU due to stalling.

Pipeline Data Hazards occur when an instruction to be executed depends on the result of a previous instruction. These occur when the pipeline alters the order of read or write access to operands, causing a different order to be observed from the order which would be present if the instructions were executed sequentially in a processor without pipelining. They negatively affect the efficiency of the CPU by causing delays and stalls.

Pipeline Structural Hazards occur due to a resource conflict. An example of this would be when more than a single instruction in the pipeline requires the exact same resource. These negatively impact the efficiency of the CPU as the instructions must be executed in series as opposed to parallel, which takes a greater amount of time.

Q.4

The AMBA (Advanced Microcontroller Bus Architecture) APB (Advanced Peripheral Bus) protocol relates a signal transition to the rising edge of the clock. This is in order to simplify the integration of APB peripherals into any design flow. Two cycles (setup and access phases) are required for every transfer. The APB protocol is not pipelined. It is used to connect to low-bandwidth peripherals which do not require very high performance. Its advantages include being a low-cost, low complexity interface which is optimized for minimal power consumption. Its disadvantages include the fact that there is only a single master which limits parallelism, scalability is poor as performance suffers as the bus is loaded, and there is poor throughput and a bottleneck in performance when multi-threading.

The AMBA AHB (Advanced High-performance Bus) specification defines an interface which is most widely used among Cortex-M processors for embedded designs and with other low latency SoCs. It is designed for high clock frequency and high performance. AHB also supports the efficient connection of processors, on-chip memories and off chip external memory interfaces. AHB involves a pipelined operation, multiple bus masters, split transactions, burst transfers, a single clock edge operation, a single cycle bus master handover and wide data bus configurations. Advantages of AMBA AHB include high performance, high bandwidth, low latency, low power consumption, ease of adding new blocks, support for multiple bus masters and a more inexpensive board. The disadvantages of AMBA AHB include poor scalability with additional blocks, the poor handling of multiple outstanding transactions and bandwidth bottleneck.

The AMBA AXI (Advanced Extensible Interface) specification defines a protocol to implement a high frequency, high bandwidth, high speed submicron design which is interconnected across a wide range of applications such as mobile, automotive, consumer and networking. It is also backwards compatible with previous interfaces including AHB and APB. It allows for high frequency operation without needing to use complex bridges. Some features of the AXI protocol include separate address, control and data phases. There are separate read and write channels to enable low-cost direct memory access. Unaligned data transfers are also supported. The advantages of AMBA AXI include high throughput, high performance, it is already a widely adopted interface standard and hence has a lot of support, it is also easier to integrate IP from different domains. The disadvantages of AMBA AXI include its relatively high latency and power consumption. It is also not a shared bus standard. It also has limitations with burst data. The burst must not cross the 4K boundary. With beats of information, it has similar limitations and is constrained to a max burst of 16 beats.

Q.5

In bus topologies, multiple components or devices use the same bus structure to transmit information signals to each other. It is thus known as the shared transmission medium. The capacity of this central cable is shared between the devices. Only one pair of devices can use this bus to transmit information successfully. If information is being transmitted by multiple devices over the bus simultaneously, the signals overlap and become jumbled. The advantages of the bus fabric topology include affordability, ease of configuration, reliability, no requirement for additional components, ease of adding an extension, scalability, and finally it has little to no power requirements. Some disadvantages include weak security, tolerance of faults is low as a single fault can bring down the entire network, the risk of collision increases greatly as the network grows larger, there are also many network issues such as data loss, ineffective network communication and improper termination.

Crossbar fabric topologies can be thought of as port switching. To make a connection in a crossbar fabric, a connection between an input and output port requires a cross point element which may be a mechanical, electrical, or an optical device. A cross connect has been established when a cross point element has been enabled. The advantages of crossbar include it is a non-blocking network which allows multiple input-output connections to be active simultaneously, it provides full connectivity as any permutation can be achieved, it is a very useful system in multiprocessor systems as all processors can send memory requests independently and asynchronously and it also makes maximum use of bandwidth. The disadvantages of crossbar are that the crossbar switch is a single layered switch, and at every point there is a switch when closed which connects one of the inputs to one of the outputs.

NOC (Network-on-Chip) fabric topologies offers a scalable and well-structured modular alternative to SoCs which can solve communication issues with on-chip systems. There are several NoC topologies which have been developed to help support numerous routing techniques and to serve varying chip architectural requirements. NoC-based alternatives offer high functional diversity and structural complexity with efficient on-chip communication. In NoC, a network is created within the chip rather than establishing a connection between all the IP blocks. The advantages of NoC include such characteristics as scalability, low-latency and high-bandwidth. The disadvantages of NoC include its thermal issues due to congestion at the centre of the network, several security concerns due to NoC’s immature security in comparison to its challenges, and finally NoC’s problem of dependency to integration technologies.

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